System Reset (with built-in watchdog timer)
Monolithic IC MM1096

Outline

This IC functions in a variety of CPU systems and other logic systems to generate a reset signal and reset the system accurately during momentary interruption or lowering of power supply voltage.
It also has a built-in watchdog timer for operation diagnosis. This prevents the system from running wild by generating an intermittent reset pulse during system mis-operation.

Features

1. Built-in watchdog timer
2. Low minimum operating voltage 130μA typ.
3. Low operating limit voltage V_{CC}=0.8V
4. Watchdog stop function (RCT pin)
5. Long clock monitoring time
   T_{PR} (POWER ON) : T_{WD} (clock monitoring)=1 : 5
6. Few external parts

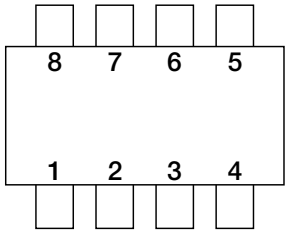
Package

DIP-8B (MM1096AD, MM1096BD)
SOP-8C (MM1096AF, MM1096BF)
SIP-8A (MM1096AS, MM1096BS)

Applications

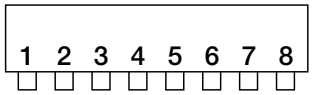
1. Reset circuits in microcomputers, CPUs and MPUs
2. Logic circuit reset circuits
3. Microcomputer system monitoring, etc.

Pin Assignment



DIP-8B/SOP-8C
(TOP VIEW)

1	TC
2	NC
3	CK
4	GND
5	V_{CC}
6	RCT
7	V_S
8	$\overline{RESET}$



SIP-8A

1	TC
2	NC
3	CK
4	GND
5	V_{CC}
6	RCT
7	V_S
8	$\overline{RESET}$

Pin Description

Pin No.	Pin name	Function
1	TC	T_{WD}, T_{WR}, T_{PR} variable pins. (T_{WD}, T_{WR} and T_{PR} times are determined by the external capacitor.) T_{PR} (ms) = 500×C_T (μF) T_{WD} (ms) = 2500×C_T (μF) T_{WR} (ms) = 100×C_T (μF)
2	N.C	
3	CK	Clock input pin, inputs clock from logic system
4	GND	GND pin
5	V_{CC}	Voltage detection MM1096A→3.2V, MM1096B→4.2V
6	RCT	Watchdog timer stop pin Operation modes : Operation→OPEN, Stop→connect to GND
7	Vs	Detection voltage variable pin
8	$\overline{\text{RESET}}$	Reset output pin (low output)

Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	V_{CC} max.	−0.3~+10	V
CK pin input voltage	V_{CK}	−0.3~V_{CC}+0.3 (≦+10)	V
Vs pin input voltage	V_{VS}	−0.3~V_{CC}+0.3 (≦+10)	V
Voltage applied to RCT pin	V_{RCT}	−0.3~V_{CC}+0.3 (≦+10)	V
Voltage applied to $\overline{\text{RESET}}$ pin	V_{OH}	−0.3~V_{CC}+0.3 (≦+10)	V
Allowable loss	Pd	300	mW
Storage temperature	T_{STG}	−40~+125	℃

Recommended Operating Conditions

Item	Symbol	Rating	Units
Power supply voltage	V_{CC}	+2.2~+7.0	V
$\overline{\text{RESET}}$ sync current	I_{OL}	0~1.0	mA
Clock monitoring time setting	T_{WD}	0.1~1000	ms
Clock rise and fall times	t_{FC}, t_{RC}	<100	μs
TC pin capacitance	C_T	0.0002~2	μF
Operating temperature	T_{OP}	−25~+75	℃

Electrical Characteristics (DC)

(Except where noted otherwise, MM1096A : V_{CC}=3.6V, Ta=25°C, MM1096B : V_{CC}=5.0V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current	MM1096A	I_{CC}	During watchdog timer operation		100	150	µA
	MM1096B				130	195	
Detection voltage	MM1096A	V_{SL}	V_S=OPEN, V_{CC} ↘	3.10	3.20	3.30	V
	MM1096B			4.05	4.20	4.35	
	MM1096A	V_{SH}	V_S=OPEN, V_{CC} ↗	3.15	3.25	3.35	
	MM1096B			4.15	4.30	4.45	
Detection voltage temperature coefficient		$V_S/\Delta T$			±0.01		%/°C
Hysteresis voltage	MM1096A	V_{HYS}	V_{SH}–V_{SL}, V_{CC} ↗↘	25	50	100	mV
	MM1096B			50	100	150	
CK input threshold		V_{TH}		0.8	1.2	2	V
CK input current		I_{IH}	A : V_{CK}=3.6V, B : V_{CK}=5.0V		0	1	µA
		I_{IL}	V_{CK}=0V	–12	–6	–2	
Output voltage (High)	MM1096A	V_{OH}	$I_{\overline{RESET}}$ =1µA	3.0	3.4		V
	MM1096B		V_S=OPEN	4.0	4.5		
Output voltage (Low)		$V_{OL}1$	$I_{\overline{RESET}}$ =0.5mA, V_S=0V		0.2	0.4	V
		$V_{OL}2$	$I_{\overline{RESET}}$ =1.0mA, V_S=0V		0.3	0.5	
R output sync current		I_{OL}	$V_{\overline{RESET}}$ =1.0V, V_S=0V	1	2		mA
C_T charge current		$I_{CT}1$	V_{TC}=1.0V during watchdog timer operation	–0.28	–0.48	–0.96	µA
		$I_{CT}2$	V_{TC}=1.0V during power ON reset operation	–1.60	–2.40	–4.80	µA
Minimum operating power supply voltage to ensure $\overline{RESET}$		V_{CCL}	$V_{\overline{RESET}}$ =0.4V $I_{\overline{RESET}}$ =0.1mA		0.8	1.0	V

Electrical Characteristics (DC)

(Except where noted otherwise, MM1096A : V_{CC}=3.6V, Ta=25°C, MM1096B : V_{CC}=5.0V)
(Except where noted otherwise, resistance unit is Ω)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V_{CC} input pulse width	MM1096A	T_{PI}	V_{CC} 3.6V / 2.8V	8			µs
	MM1096B		V_{CC} 5.0V / 4.0V	8			
CK input pulse width		T_{CKW}	CK or	3			µs
CK input cycle		T_{CK}		20			µs
Watchdog timer monitoring time *1		T_{WD}	C_T=0.02µF	25	50	75	ms
Reset time for watchdog timer *2		T_{WR}	C_T=0.02µF	1	2	3	ms
Reset hold time for power supply rise *3		T_{PR}	C_T=0.02µF, V_{CC}	5	10	15	ms
Output delay time from V_{CC} *4		T_{PD}	$\overline{RESET}$ pin, R_L=10k, C_L=20pF		2	10	µs
Output rise time *5		t_R	$\overline{RESET}$ pin, R_L=10k, C_L=20pF		2.0	4.0	µs
Output fall time *5		t_F	$\overline{RESET}$ pin, R_L=10k, C_L=20pF		0.2	1.0	µs

Notes:

*1 Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse until reset pulse output. In other words, reset output is output if a clock pulse is not input during this time.

*2 Reset time means reset pulse width. However, this does not apply to power ON reset.

*3 Reset hold time is the time from when V_{CC} exceeds detection voltage (V_{SH}) during power ON reset until reset release ($\overline{RESET}$ output high).

*4 Output delay time is the time from when power supply voltage drops below detection voltage (V_{SL}) until reset ($\overline{RESET}$ output low).

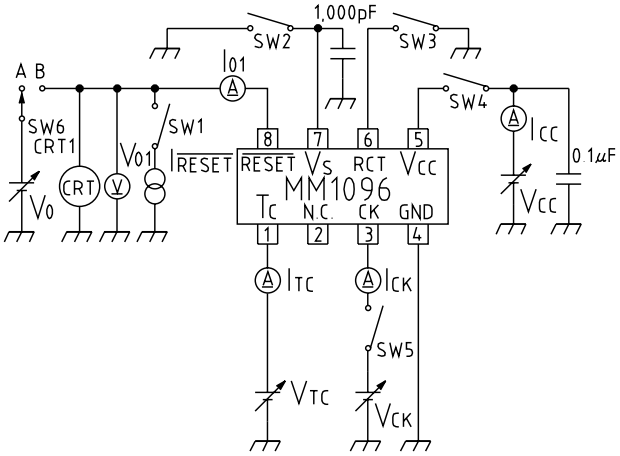
*5 Voltage range when measuring output rise and fall is 10~90%.

*6 Watchdog timer monitoring time (T_{WD}), watchdog timer reset time (T_{WR}) and reset hold time (T_{PR}) during power supply rise can be changed by varying C_T capacitance. The times are expressed by the following formulae.

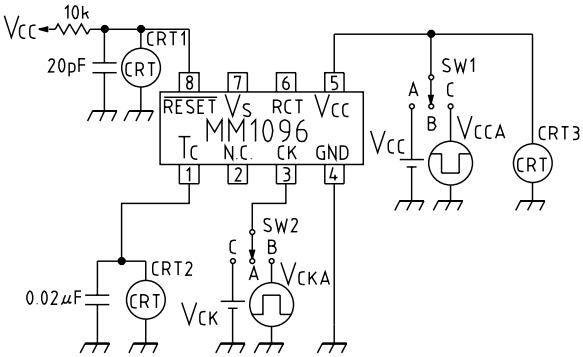
T_{PR} (ms) ≒ 500 × C_T (µF)
T_{WD} (ms) ≒ 2500 × C_T (µF)
T_{WR} (ms) ≒ 100 × C_T (µF)
Example : When C_T=0.02µF
T_{PR} ≒ 10ms
T_{WD} ≒ 50ms
T_{WR} ≒ 2ms

Measuring Circuits

Measuring Circuit 1 (DC)



Measuring Circuit 2 (AC)



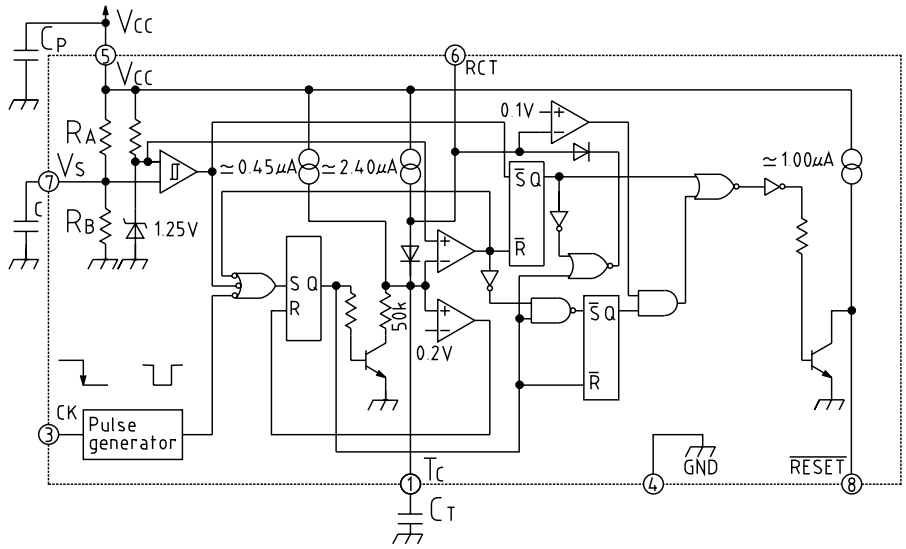
Measuring Circuit 1 SW & Power Supply Table

Item	Symbol	SW1	SW2	SW3	SW4	SW5	SW6	VCC	VCK	VCT	IRESET	VM, IM	Notes
Consumption current	ICC	OFF	OFF	OFF	ON	ON	A	3.6V	3.6V	0V		ICC	
Detection voltage	VSL	OFF	OFF	ON	ON	ON	A	3.6V→3V	0V	2V		VO1, CRT1	
	VSH	OFF	OFF	ON	ON	ON	A	3V→3.6V	0V	2V		VO1, CRT1	
CK input threshold	VTH	OFF	OFF	OFF	ON	ON	A	3.6V	0V→3V	1V		ICK, VCK	
CK input current	IIH	OFF	OFF	OFF	ON	ON	A	3.6V	3.6V	0V		ICK	
	IIL	OFF	OFF	OFF	ON	ON	A	3.6V	0V	0V		ICK	
Output voltage (High)	VOH	ON	OFF	ON	ON	ON	A	3.6V	3.6V	2V	−1μA	VO1	
Output voltage (Low)	VOL1	ON	ON	ON	ON	ON	A	3.6V	3.6V	2V	0.5mA	VO1	
	VOL2	ON	ON	ON	ON	ON	A	3.6V	3.6V	2V	1.0mA	VO1	
Output sink current	IOL1	OFF	ON	ON	ON	ON	B	3.6V	3.6V	2V		IO1	VO=1V
CT charge current 1	ITC1	OFF	OFF	OFF	ON	OFF	A	3.6V		1V		ITC	
CT charge current 2	ITC2	OFF	OFF	OFF	ON	OFF	A	3.6V		IV		ITC	
Minimum operating power supply voltage to ensure RESET	VCCL	ON	OFF	ON	ON	ON	A	0V→2V	0V	0V		VO1, VCC	

Measuring Circuit 2 SW & Power Supply Table

Item	Symbol	SW1	SW2	VCCA	VCC	VCKA	VCK	CRT	Notes
VCC input pulse width	TP1	C	B	3.6V / 2.8V, T1	−	1.4V / 0V, T2, T3	−	CRT1 CRT2	T1=8μs
CK input pulse width	TCKW	A	B	−	3.6V	1.4V / 0V, T2 or T2	−	CRT1 CRT2	T2=3μs
CK input cycle	TCK	A	B	−	3.6V	1.4V / 0V, T2, T3	−	CRT1 CRT2	T3=20μs
Watchdog timer monitoring time	TWD	A	A	−	3.6V	−	3.6V	CRT1 CRT2	
Reset time for watchdog timer	TWR	A	A	−	3.6V	−	3.6V	CRT1 CRT2	
Reset hold time for power supply rise	TPR	B→A	A	−	3.6V	−	3.6V	CRT1 CRT2	
Output delay time from VCC	TPD	C	A	3.6V / 0V	−	−	0V	CRT1	
Output rise time	TR	A	A	−	3.6V	−	3.6V	CRT1	
Output fall time	TF	A	A	−	3.6V	−	3.6V	CRT1	

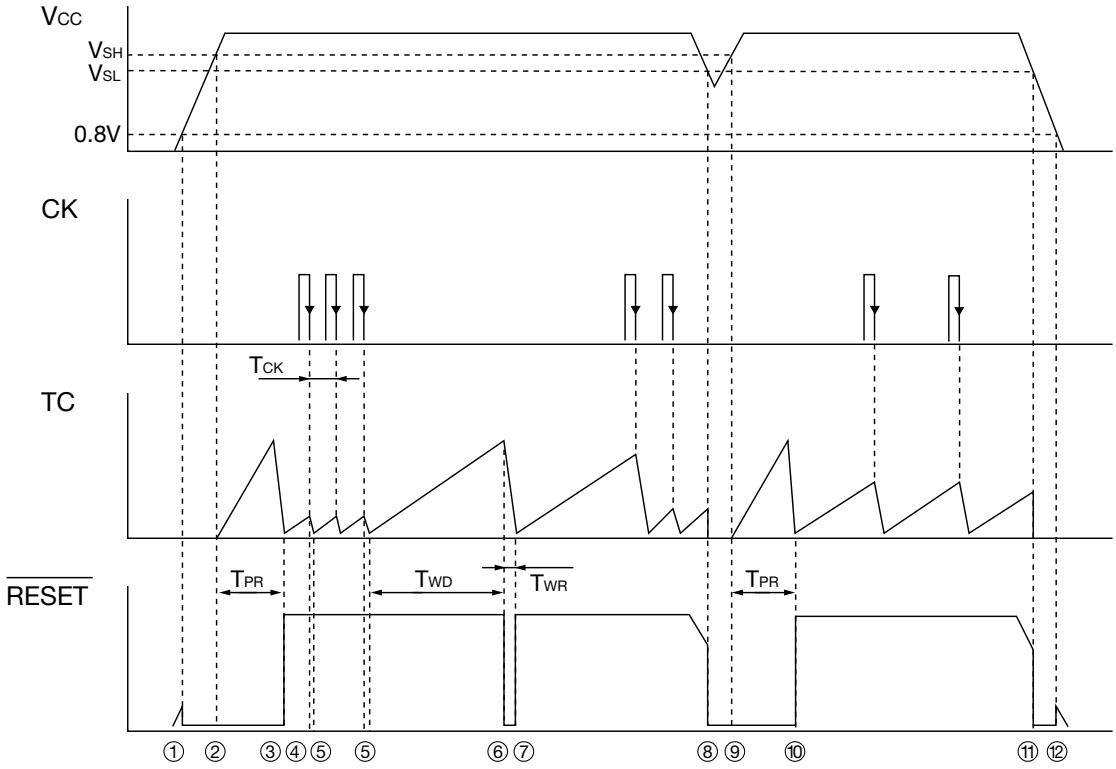
Block Diagram



	RA	RB
MM1096A	≃305k	≃195k
MM1096B	≃350k	≃150k

Note 1: CP=0.1μF approx.
Note 2: C ≧ 1000pF
Note 3: The watchdog timer can be stopped by connecting the RCT pin to GND. Then it functions as a voltage detection circuit.)

Timing Chart



Description of Operation

1. $\overline{\text{RESET}}$ goes low when V_{CC} rises to approximately 0.8V.
   Approximately 1μA (V_{CC}=0.8V) of pull up current is output from $\overline{\text{RESET}}$
2. Capacitor C_T charging starts when V_{CC} rises to V_{SH} (MM1096A ≒ 3.25V, MM1096B ≒ 4.3V). Output is in reset state at this time.
3. Output reset is released ($\overline{\text{RESET}}$ goes high) after a certain time (T_{PR}), from when C_T starts charging until discharge (the time from when C_T voltage reaches a certain threshold value 1 (≒ 1.4V) until C_T voltage drops to a certain threshold value 2 (≒ 0.2V).
   Reset hold time : T_{PR} is as follows.
   T_{PR} (ms) ≒ 500 × C_T (μF)
   C_T charging starts again after reset release, and watchdog timer operation begins.
   Clock input to the CK pin during C_T charging will cause mis-operation.
4. If a clock is input (negative edge trigger) to the CK pin during C_T charging, C switches from charging to discharge.
5. Discharge switches to charging when C_T voltage drops to a certain threshold value (≒ 0.2V). Steps 4 and 5 are repeated while a normal clock is input from the logic system.
6. Output goes to reset state ($\overline{\text{RESET}}$ goes low) when the clock ceases and C_T voltage reaches reset ON threshold value (≒ 1.4V).
   The formula for C_T charging time (T_{WD} : watchdog timer monitoring time) until reset is output is as follows.
   T_{WD} (ms) ≒ 2500 × C_T (μF)
7. Watchdog timer reset time T_{WR} is the discharge time until C_T voltage drops to reset OFF threshold value (≒ 0.2V). The formula is as follows.
   T_{WR} (ms) ≒ 100 × C_T (μF)
   After reset OFF threshold value is reached, output reset is released and C_T starts charging. Thereafter, steps 4 and 5 are repeated if a normal clock is input, and when the clock ceases, 6 and 7 are repeated.
8. Reset is output when V_{CC} drops to V_{SL} (MM1096A ≒ 3.2V, MM1096B ≒ 4.2V). C_T is charged simultaneously.
9. C_T charging starts when V_{CC} rises to V_{SH}.
   When V_{CC} drops momentarily, C_T charging begins after the charge is first discharged, if the time from V_{CC} dropping below V_{SL} until it rises to V_{SH} is longer than the Vcc input pulse width standard value T_{PI}.
10. Output reset is released after V_{CC} goes above V_{SH} and after T_{PR}, and the watchdog timer starts. Thereafter, 8~10 are repeated when V_{CC} goes below V_{SL}.
11. When power is OFF, reset is output if V_{CC} goes below V_{SL}.
12. When V_{CC} drops to 0V, reset output is held until V_{CC} reaches 0.8V.